Fig. 1 PRIOR ART

PACKAGE TYPE	TSOP	CSP	PRODUCT SPECIFICATIONS Max/Min
TERMINAL CAPACITANCE IN PACKAGE	1.00	0.14	3.50/2.50

Fig. 2A PRIOR ART

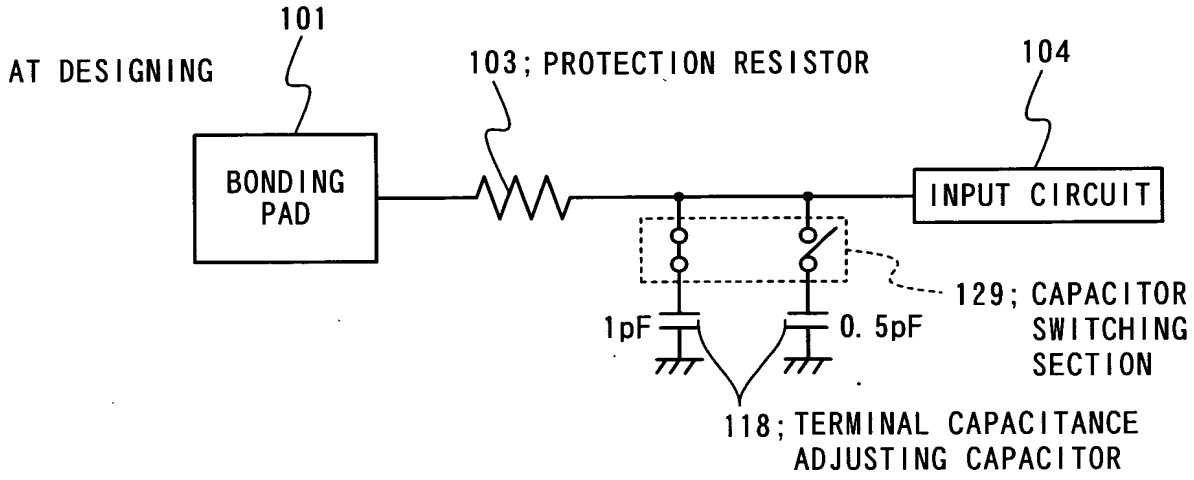


Fig. 2B PRIOR ART

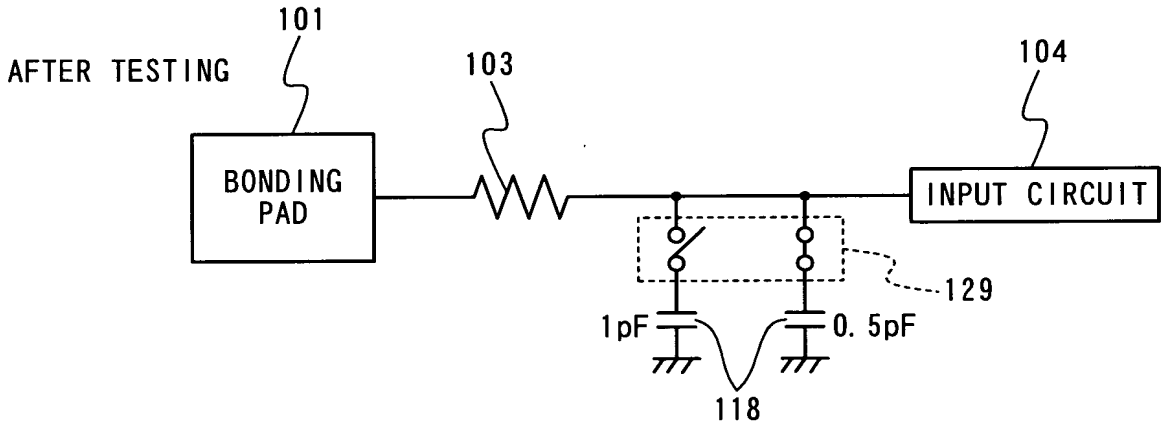


Fig. 3 PRIOR ART

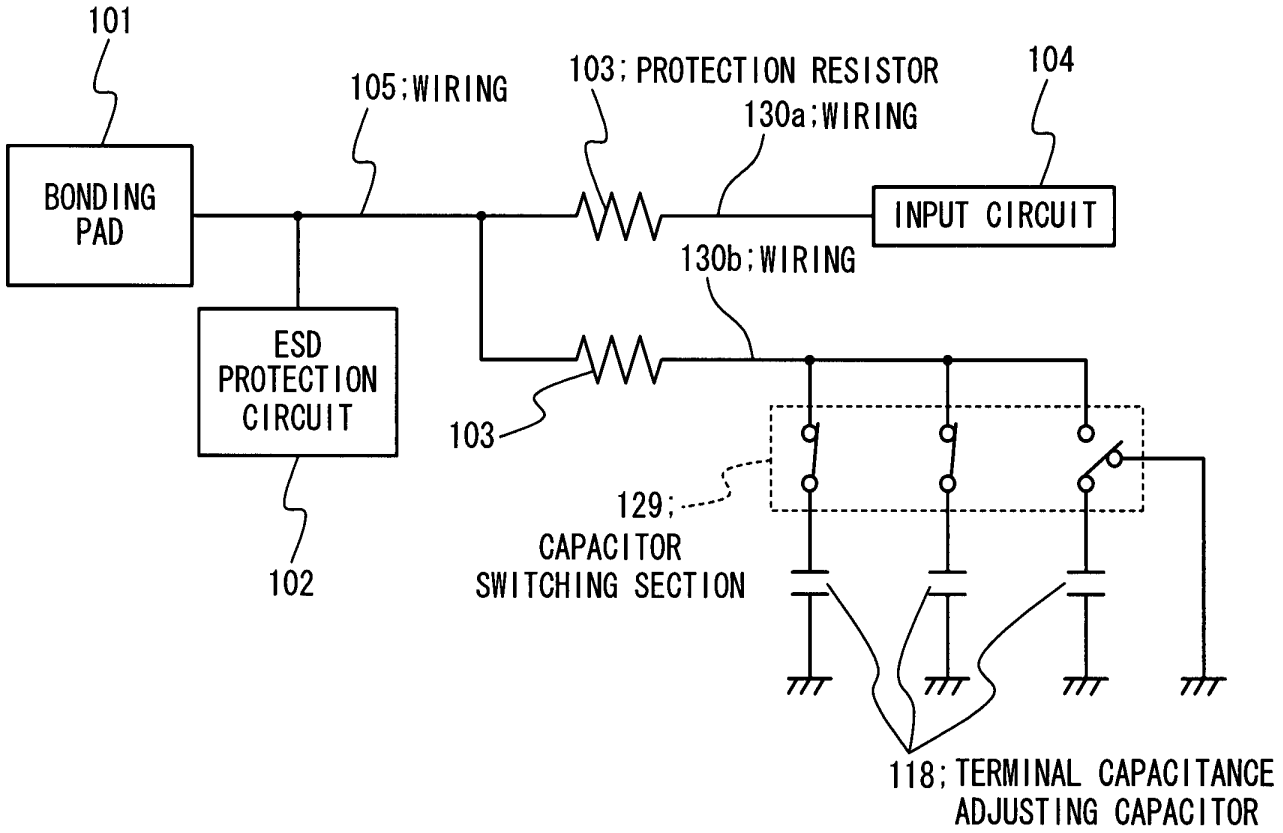


Fig. 4 PRIOR ART

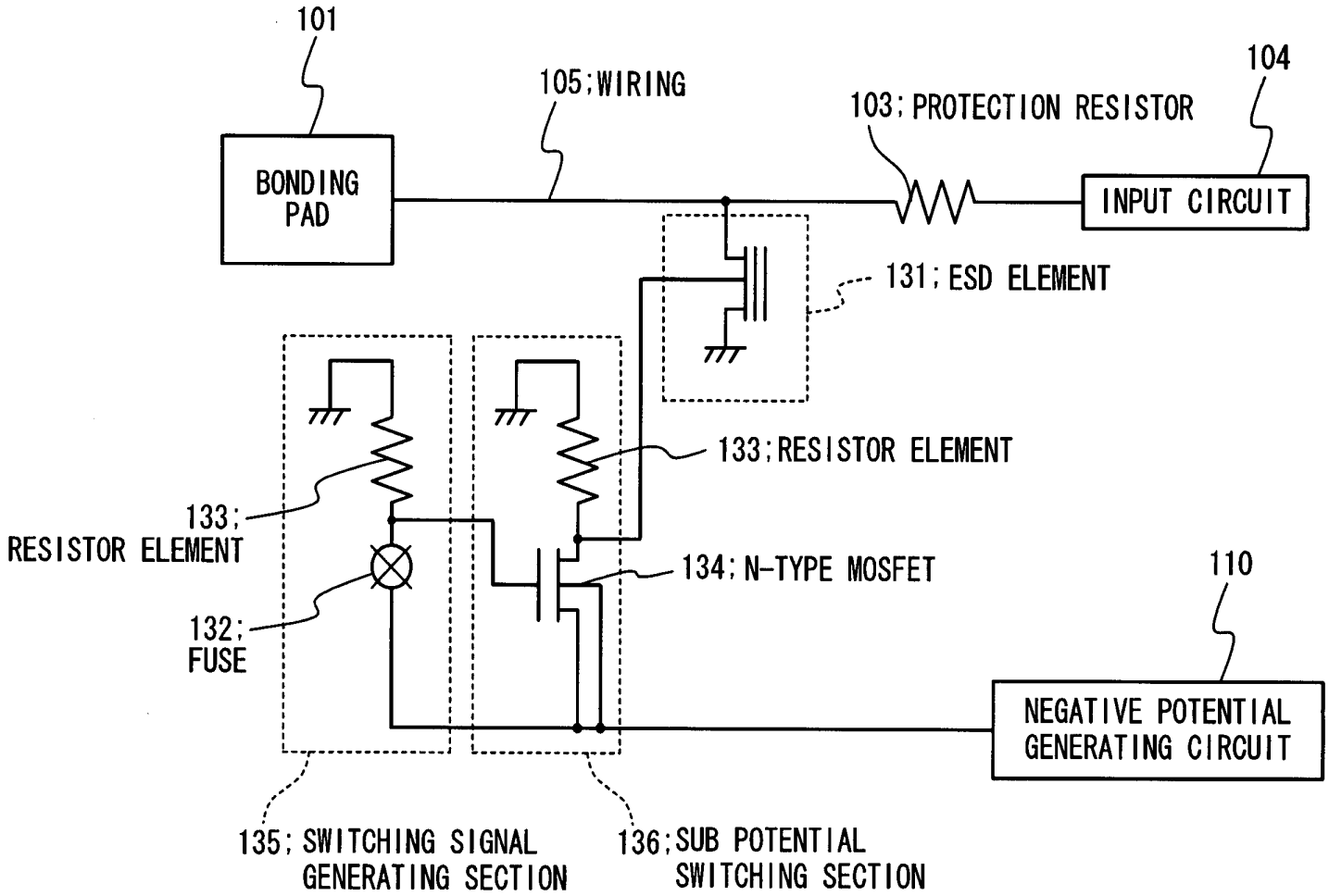


Fig. 5A

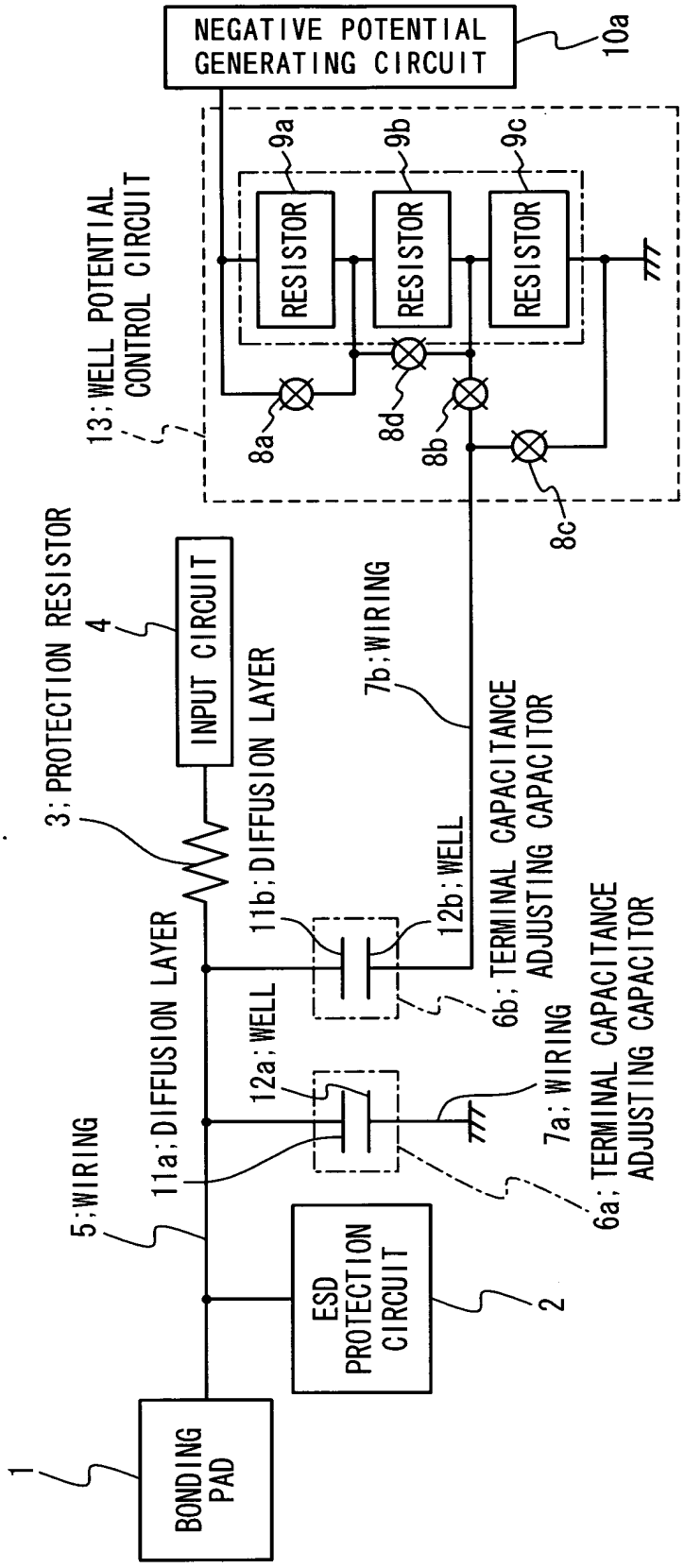

NEGATIVE POTENTIAL GENERATING CIRCUIT
10a
13; WELL POTENTIAL CONTROL CIRCUIT
9a
9b
9c
RESISTOR
RESISTOR
RESISTOR
8a
8d
8b
8c
3; PROTECTION RESISTOR
4
INPUT CIRCUIT
7b; WIRING
11b; DIFFUSION LAYER
12b; WELL
6b; TERMINAL CAPACITANCE ADJUSTING CAPACITOR
11a; DIFFUSION LAYER
12a; WELL
7a; WIRING
6a; TERMINAL CAPACITANCE ADJUSTING CAPACITOR
5; WIRING
ESD PROTECTION CIRCUIT
2
1
BONDING PAD

Fig. 5B

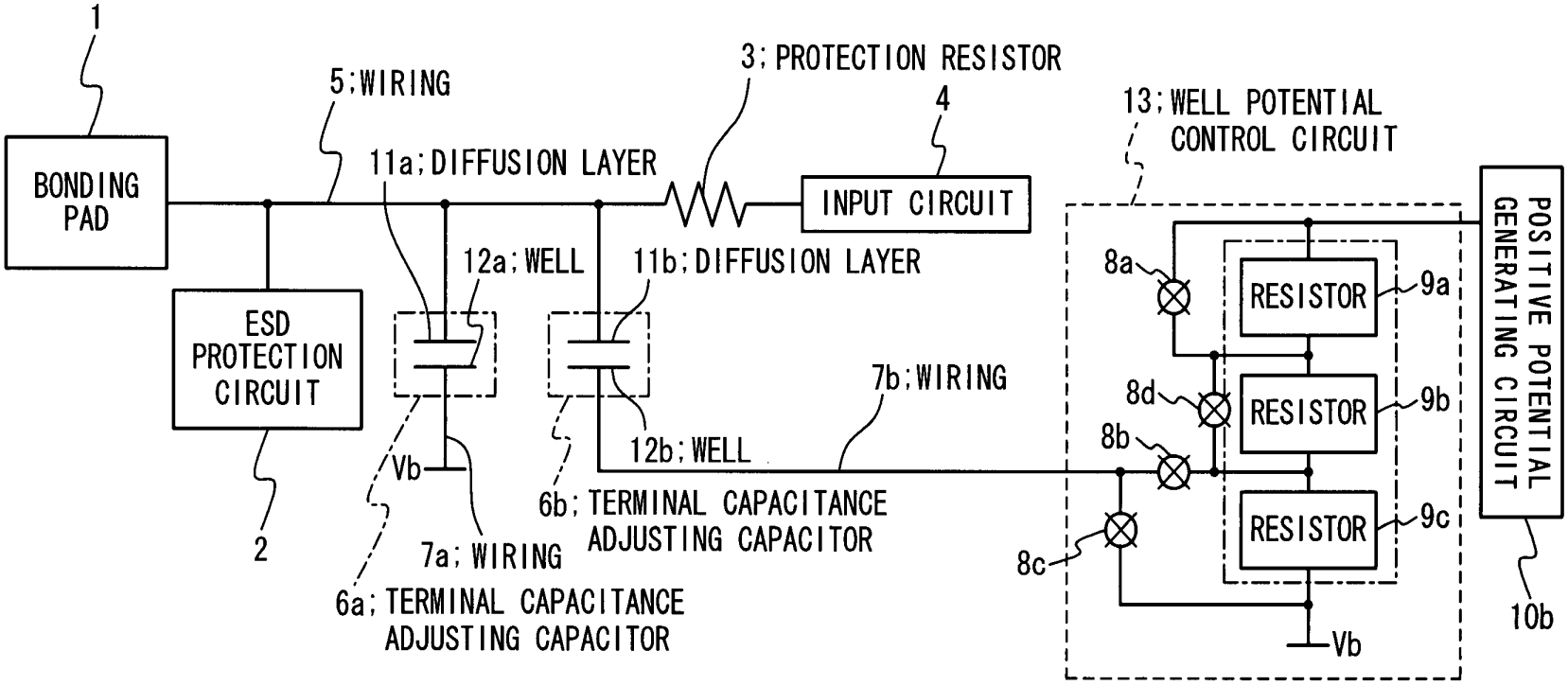

1
BONDING PAD
5;WIRING
11a;DIFFUSION LAYER
3;PROTECTION RESISTOR
4
INPUT CIRCUIT
13;WELL POTENTIAL CONTROL CIRCUIT
POSITIVE POTENTIAL GENERATING CIRCUIT
ESD PROTECTION CIRCUIT
12a;WELL
11b;DIFFUSION LAYER
7b;WIRING
8a
RESISTOR
9a
8d
RESISTOR
9b
8b
RESISTOR
9c
8c
Vb
12b;WELL
6b;TERMINAL CAPACITANCE ADJUSTING CAPACITOR
2
7a;WIRING
6a;TERMINAL CAPACITANCE ADJUSTING CAPACITOR
10b

Fig. 6

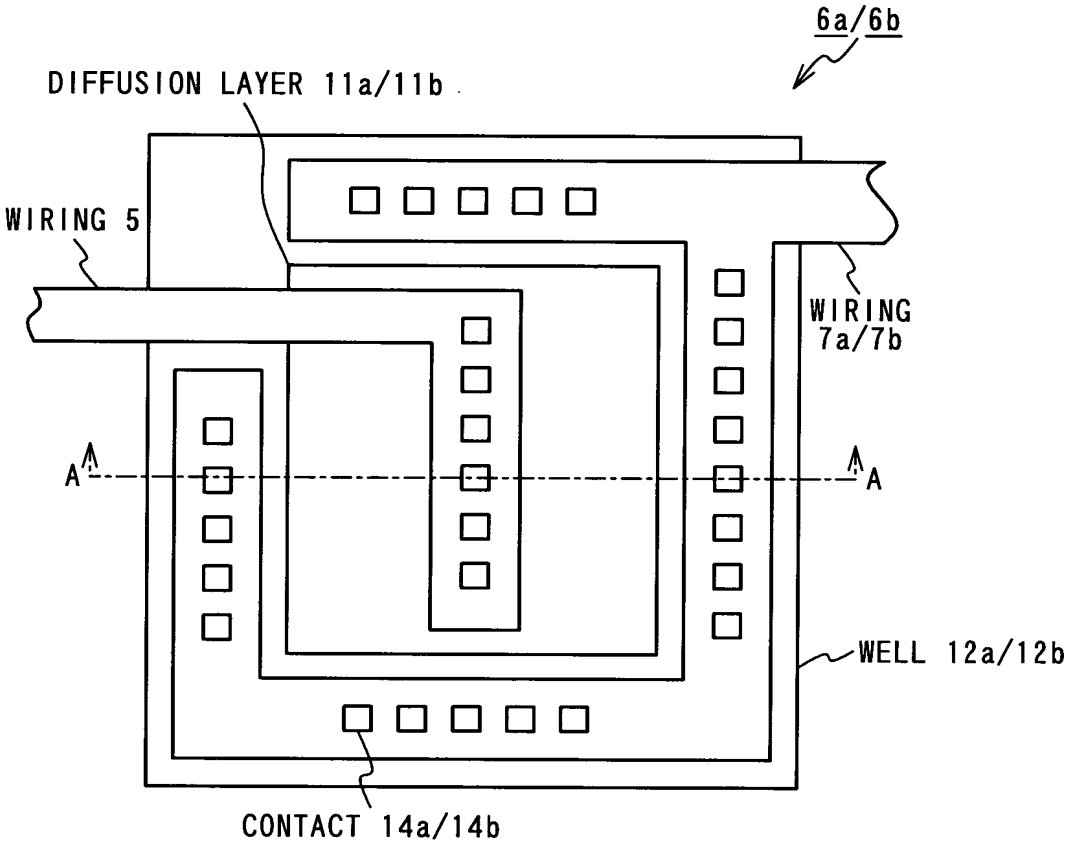

6a/6b
DIFFUSION LAYER 11a/11b
WIRING 5
WIRING
7a/7b
A
A
WELL 12a/12b
CONTACT 14a/14b

Fig. 7

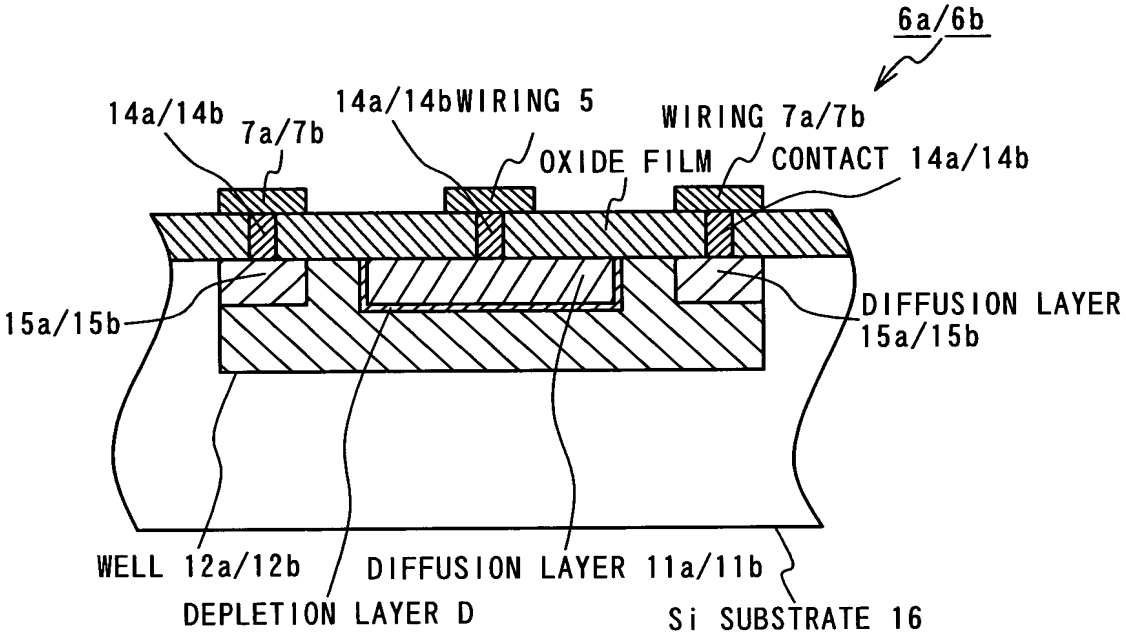

6a/6b
14a/14b
7a/7b
14a/14bWIRING 5
WIRING 7a/7b
OXIDE FILM
CONTACT 14a/14b
15a/15b
DIFFUSION LAYER
15a/15b
WELL 12a/12b
DIFFUSION LAYER 11a/11b
DEPLETION LAYER D
Si SUBSTRATE 16

Fig. 8

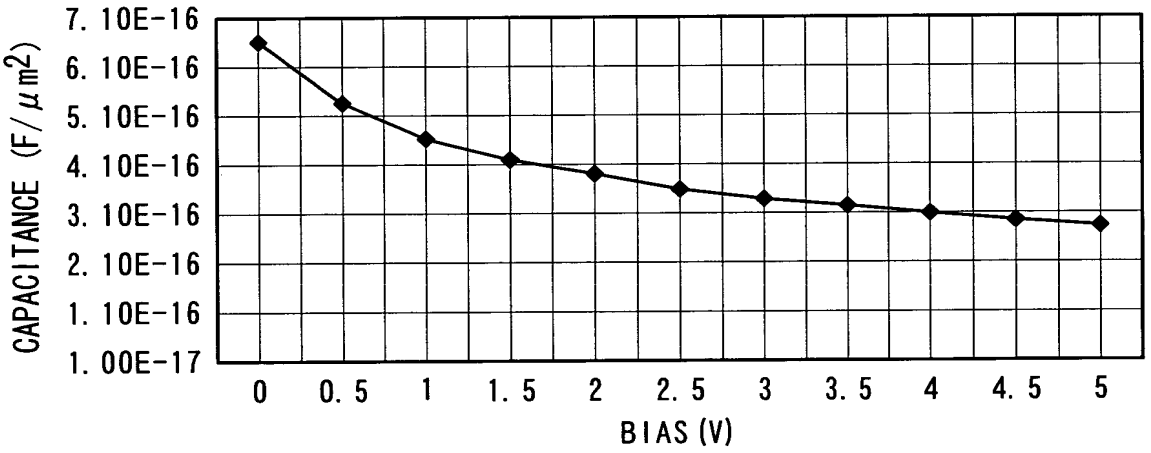

CAPACITANCE (F/μm²)
7.10E-16
6.10E-16
5.10E-16
4.10E-16
3.10E-16
2.10E-16
1.10E-16
1.00E-17
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
BIAS (V)

Fig. 9

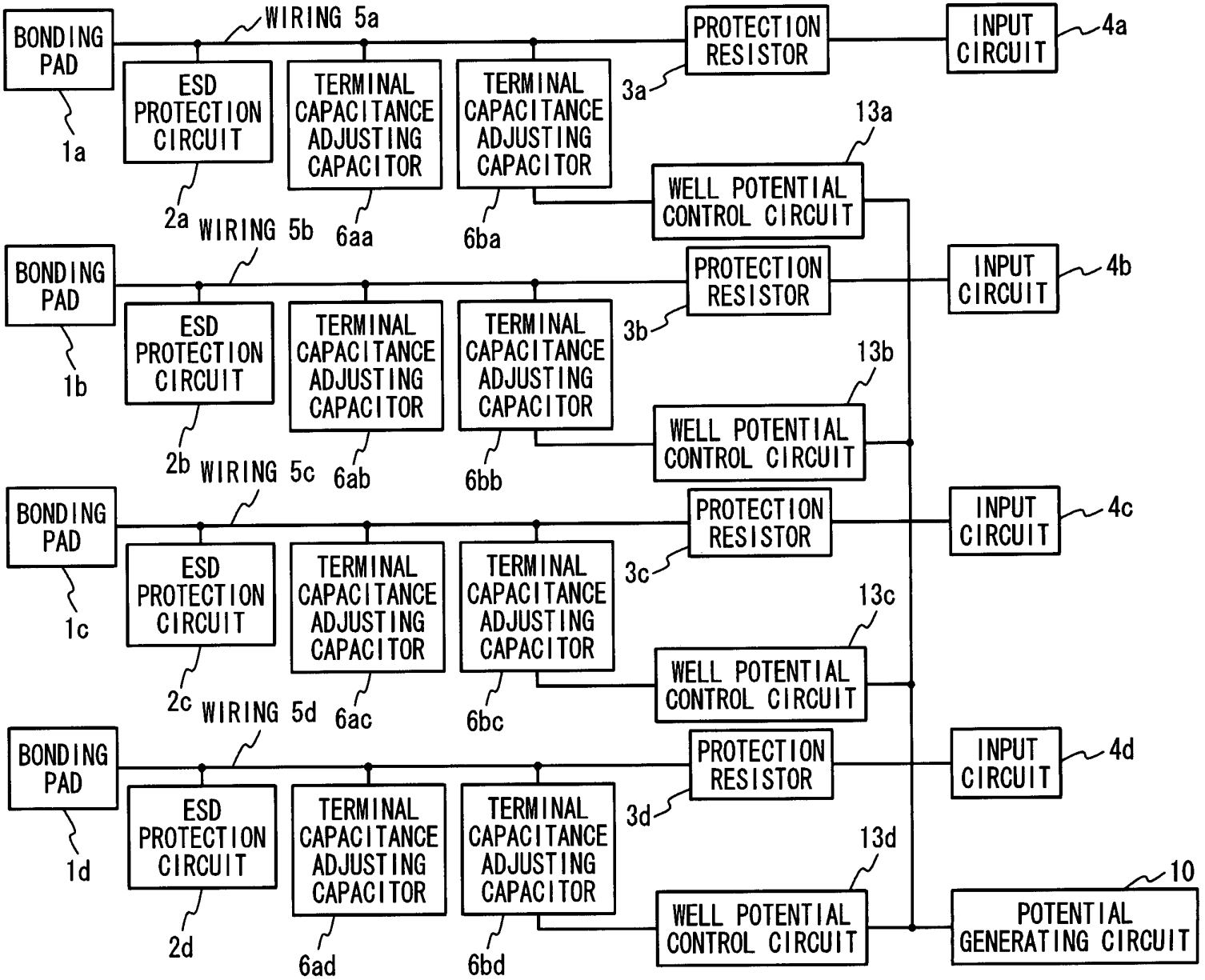

BONDING PAD
1a
WIRING 5a
ESD PROTECTION CIRCUIT
2a
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6aa
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ba
PROTECTION RESISTOR
3a
INPUT CIRCUIT
4a
13a
WELL POTENTIAL CONTROL CIRCUIT
BONDING PAD
1b
WIRING 5b
ESD PROTECTION CIRCUIT
2b
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ab
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bb
PROTECTION RESISTOR
3b
INPUT CIRCUIT
4b
13b
WELL POTENTIAL CONTROL CIRCUIT
BONDING PAD
1c
WIRING 5c
ESD PROTECTION CIRCUIT
2c
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ac
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bc
PROTECTION RESISTOR
3c
INPUT CIRCUIT
4c
13c
WELL POTENTIAL CONTROL CIRCUIT
BONDING PAD
1d
WIRING 5d
ESD PROTECTION CIRCUIT
2d
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ad
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bd
PROTECTION RESISTOR
3d
INPUT CIRCUIT
4d
13d
WELL POTENTIAL CONTROL CIRCUIT
10
POTENTIAL GENERATING CIRCUIT

Fig. 10

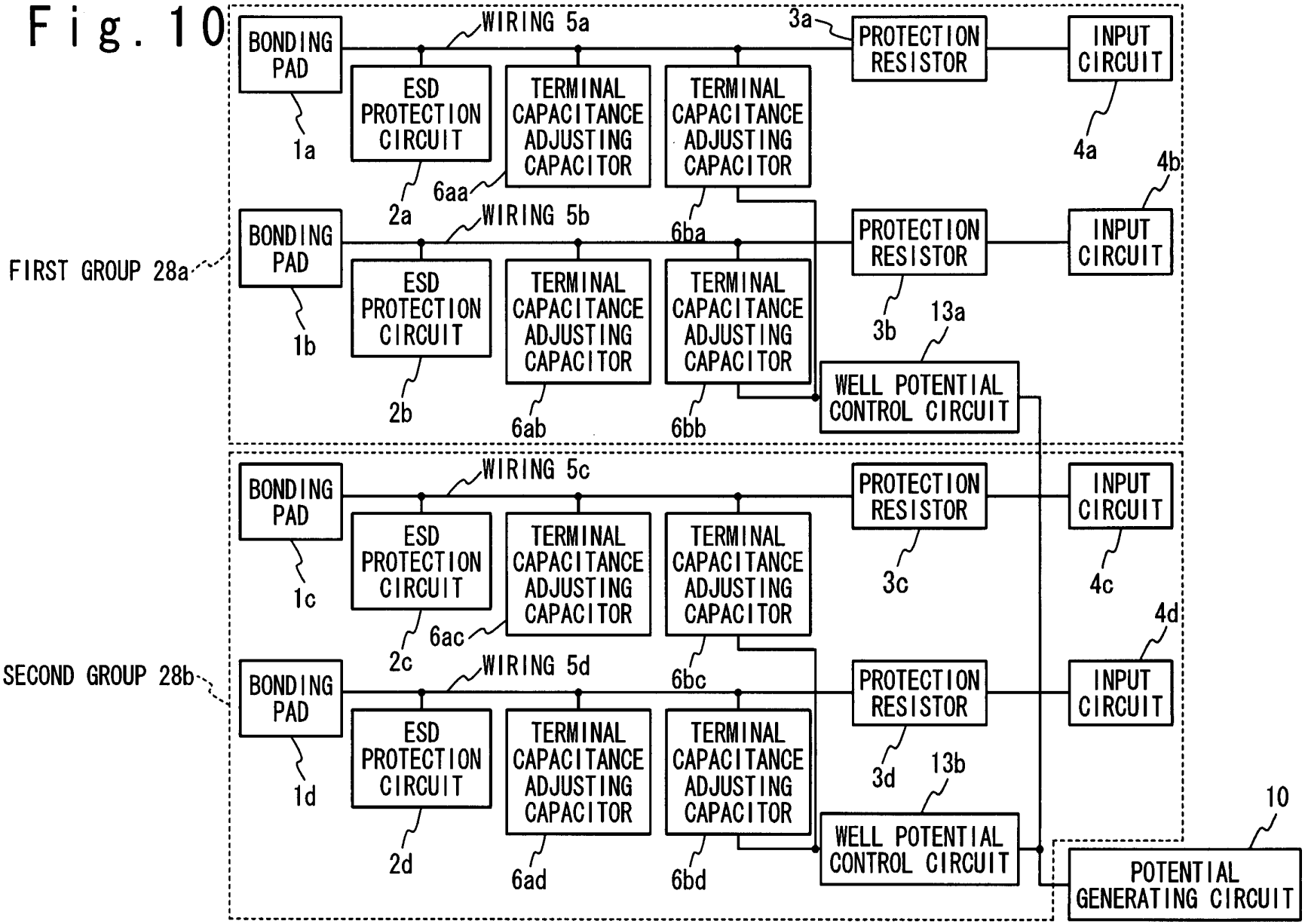

BONDING PAD
1a
ESD PROTECTION CIRCUIT
2a
WIRING 5a
6aa
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ba
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
3a
PROTECTION RESISTOR
INPUT CIRCUIT
4a
4b
FIRST GROUP 28a
BONDING PAD
1b
ESD PROTECTION CIRCUIT
2b
WIRING 5b
6ab
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bb
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
PROTECTION RESISTOR
3b
INPUT CIRCUIT
13a
WELL POTENTIAL CONTROL CIRCUIT
BONDING PAD
1c
ESD PROTECTION CIRCUIT
2c
WIRING 5c
6ac
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bc
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
PROTECTION RESISTOR
3c
INPUT CIRCUIT
4c
4d
SECOND GROUP 28b
BONDING PAD
1d
ESD PROTECTION CIRCUIT
2d
WIRING 5d
6ad
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bd
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
PROTECTION RESISTOR
3d
INPUT CIRCUIT
13b
WELL POTENTIAL CONTROL CIRCUIT
10
POTENTIAL GENERATING CIRCUIT

Fig. 11

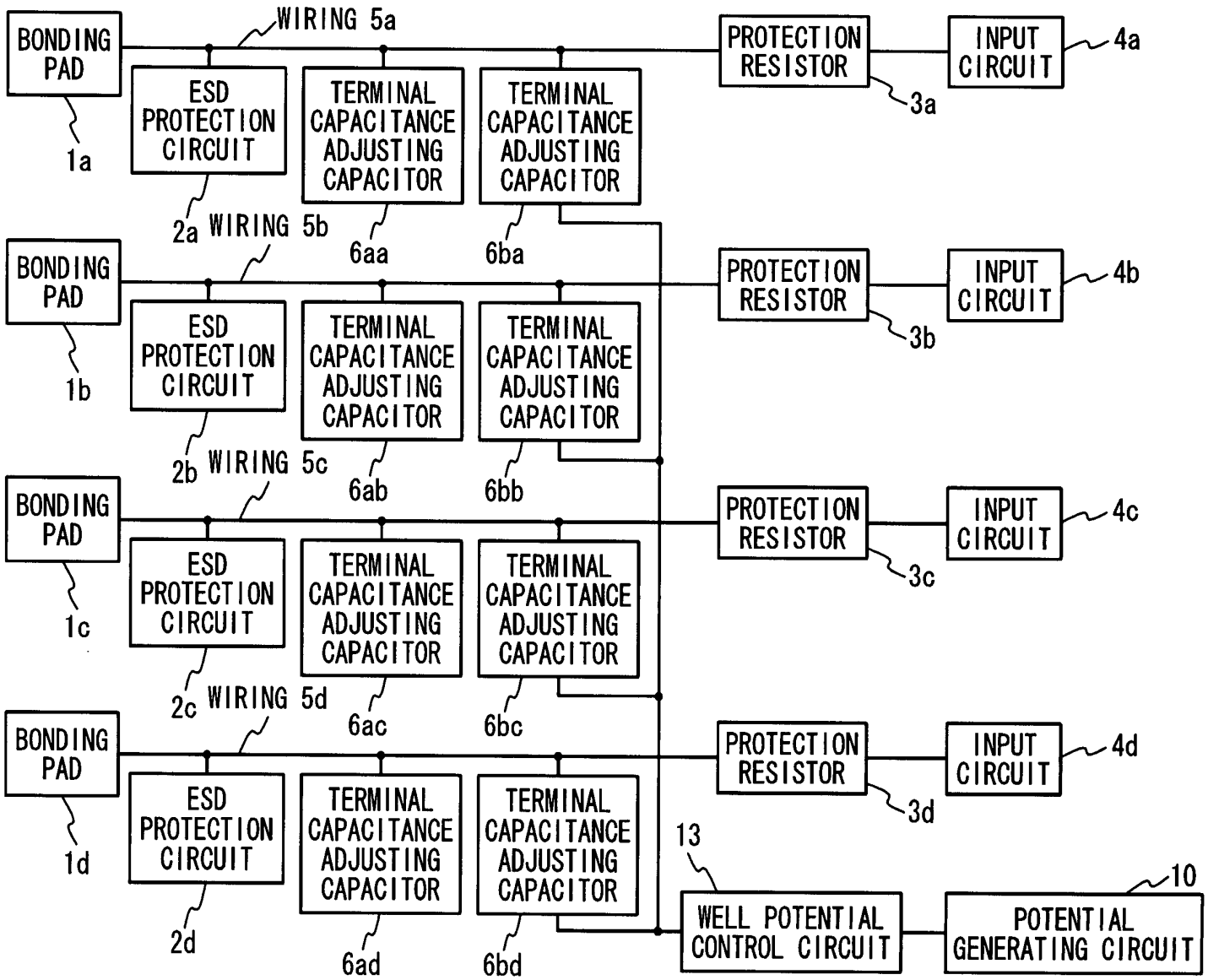

BONDING PAD
1a
ESD PROTECTION CIRCUIT
2a
WIRING 5a
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6aa
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ba
PROTECTION RESISTOR
3a
INPUT CIRCUIT
4a
BONDING PAD
1b
ESD PROTECTION CIRCUIT
2b
WIRING 5b
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ab
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bb
PROTECTION RESISTOR
3b
INPUT CIRCUIT
4b
BONDING PAD
1c
ESD PROTECTION CIRCUIT
2c
WIRING 5c
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ac
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bc
PROTECTION RESISTOR
3c
INPUT CIRCUIT
4c
BONDING PAD
1d
ESD PROTECTION CIRCUIT
2d
WIRING 5d
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ad
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bd
PROTECTION RESISTOR
3d
INPUT CIRCUIT
4d
13
WELL POTENTIAL CONTROL CIRCUIT
10
POTENTIAL GENERATING CIRCUIT

Fig. 12

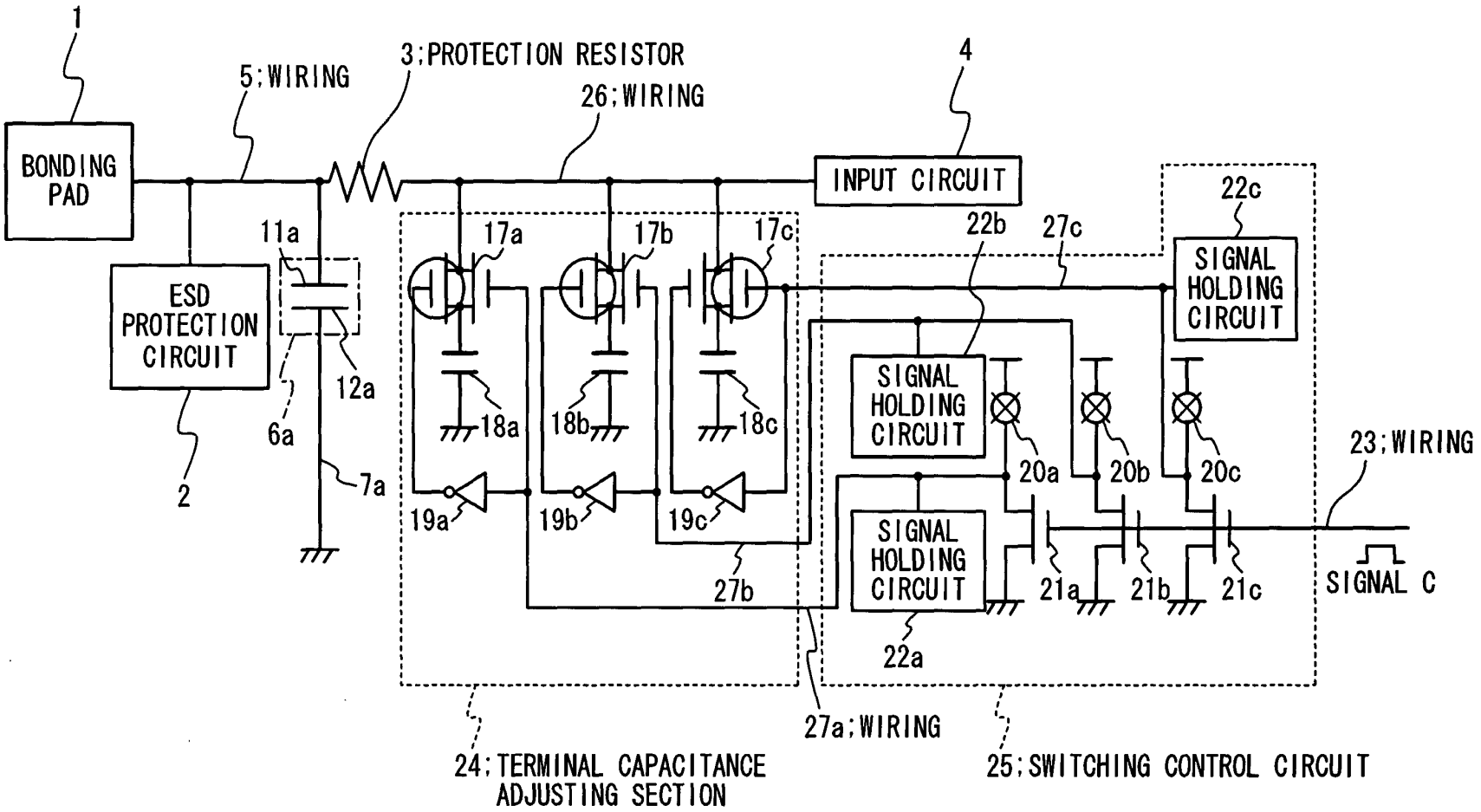

1
BONDING PAD
5;WIRING
3;PROTECTION RESISTOR
26;WIRING
4
INPUT CIRCUIT
ESD PROTECTION CIRCUIT
2
11a
6a
12a
7a
17a
17b
17c
18a
18b
18c
19a
19b
19c
27b
22b
27c
22c
SIGNAL HOLDING CIRCUIT
SIGNAL HOLDING CIRCUIT
SIGNAL HOLDING CIRCUIT
22a
20a
20b
20c
21a
21b
21c
23;WIRING
SIGNAL C
27a;WIRING
24;TERMINAL CAPACITANCE ADJUSTING SECTION
25;SWITCHING CONTROL CIRCUIT

Fig. 13

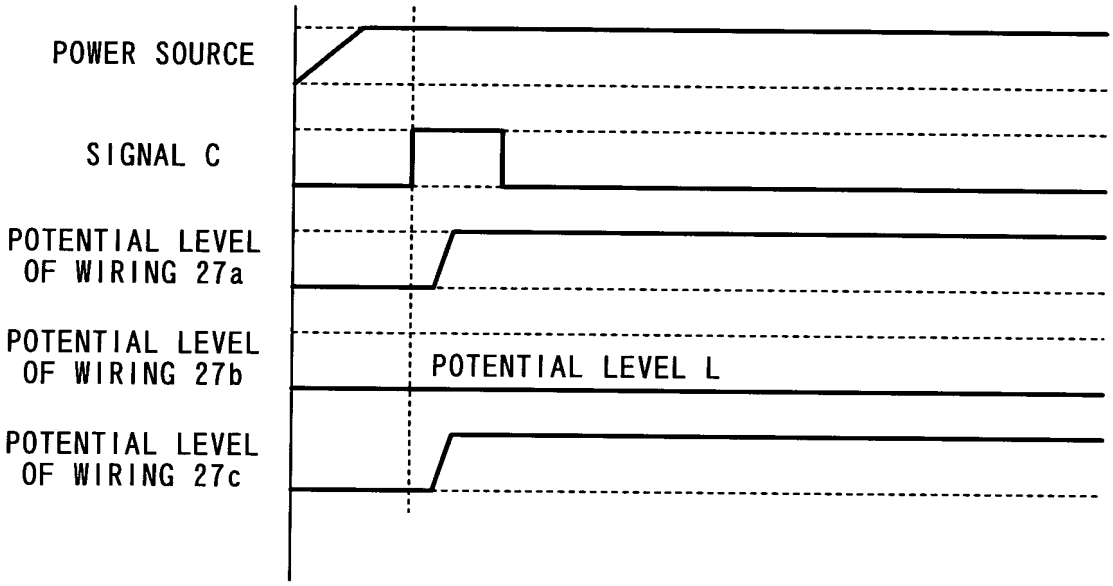

POWER SOURCE
SIGNAL C
POTENTIAL LEVEL OF WIRING 27a
POTENTIAL LEVEL OF WIRING 27b
POTENTIAL LEVEL L
POTENTIAL LEVEL OF WIRING 27c

Fig. 14

	1	2	3	4	5	6	7	8
FUSE 20a	○	×	×	○	○	○	×	×
FUSE 20b	○	○	×	○	×	×	○	×
FUSE 20c	○	○	○	×	×	○	×	×
TOTAL TERMINAL CAPACITANCE	3pF	2pF	0pF	6pF	4pF	1pF	5pF	3pF

Fig. 15

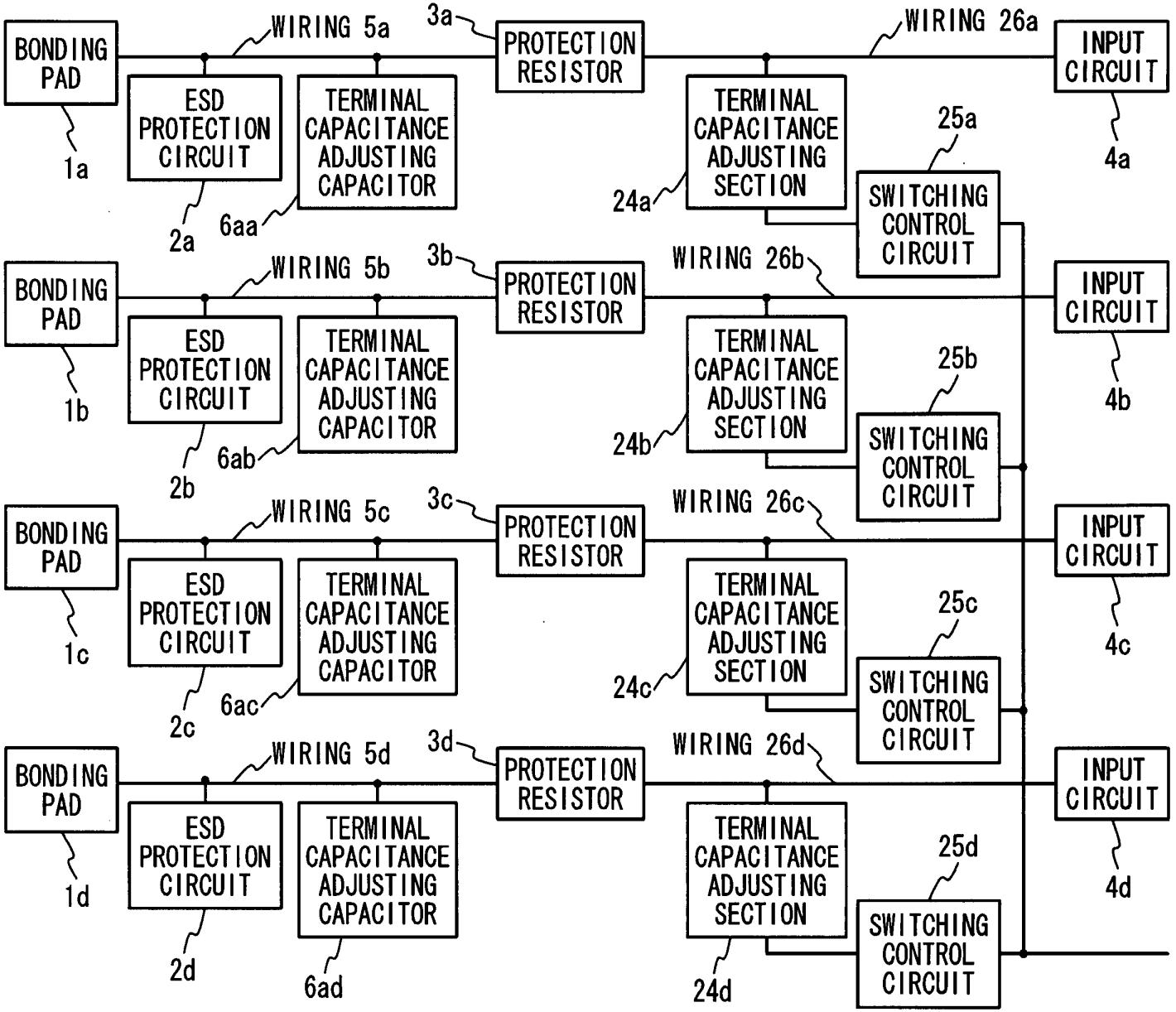

BONDING PAD
1a
WIRING 5a
ESD PROTECTION CIRCUIT
2a
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6aa
3a
PROTECTION RESISTOR
WIRING 26a
TERMINAL CAPACITANCE ADJUSTING SECTION
24a
25a
SWITCHING CONTROL CIRCUIT
INPUT CIRCUIT
4a
BONDING PAD
1b
WIRING 5b
ESD PROTECTION CIRCUIT
2b
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ab
3b
PROTECTION RESISTOR
WIRING 26b
TERMINAL CAPACITANCE ADJUSTING SECTION
24b
25b
SWITCHING CONTROL CIRCUIT
INPUT CIRCUIT
4b
BONDING PAD
1c
WIRING 5c
ESD PROTECTION CIRCUIT
2c
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ac
3c
PROTECTION RESISTOR
WIRING 26c
TERMINAL CAPACITANCE ADJUSTING SECTION
24c
25c
SWITCHING CONTROL CIRCUIT
INPUT CIRCUIT
4c
BONDING PAD
1d
WIRING 5d
ESD PROTECTION CIRCUIT
2d
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ad
3d
PROTECTION RESISTOR
WIRING 26d
TERMINAL CAPACITANCE ADJUSTING SECTION
24d
25d
SWITCHING CONTROL CIRCUIT
INPUT CIRCUIT
4d

Fig. 16

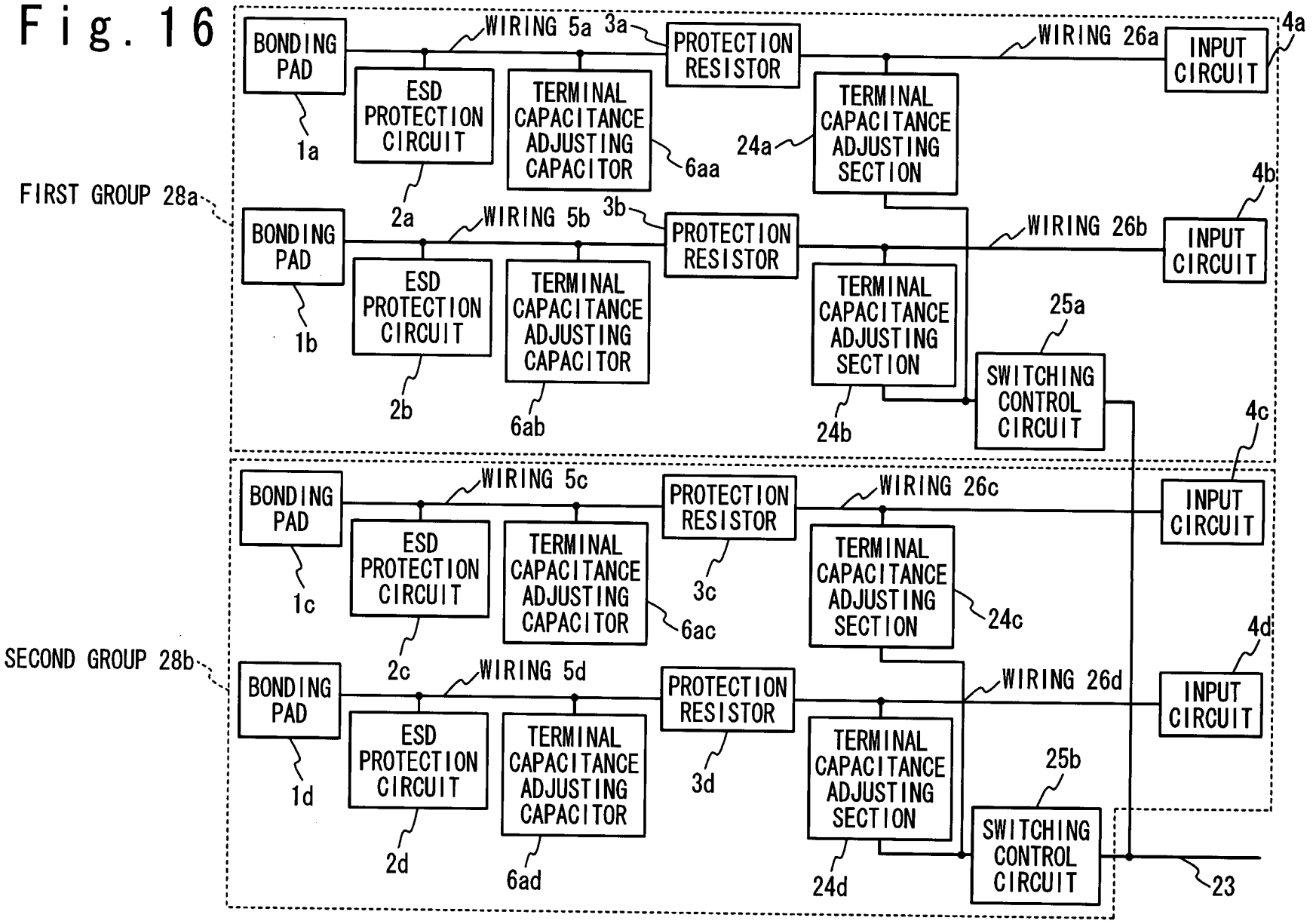

FIRST GROUP 28a
SECOND GROUP 28b
BONDING PAD
1a
1b
1c
1d
ESD PROTECTION CIRCUIT
2a
2b
2c
2d
WIRING 5a
WIRING 5b
WIRING 5c
WIRING 5d
3a
3b
3c
3d
PROTECTION RESISTOR
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6aa
6ab
6ac
6ad
TERMINAL CAPACITANCE ADJUSTING SECTION
24a
24b
24c
24d
WIRING 26a
WIRING 26b
WIRING 26c
WIRING 26d
INPUT CIRCUIT
4a
4b
4c
4d
SWITCHING CONTROL CIRCUIT
25a
25b
23

Fig. 17

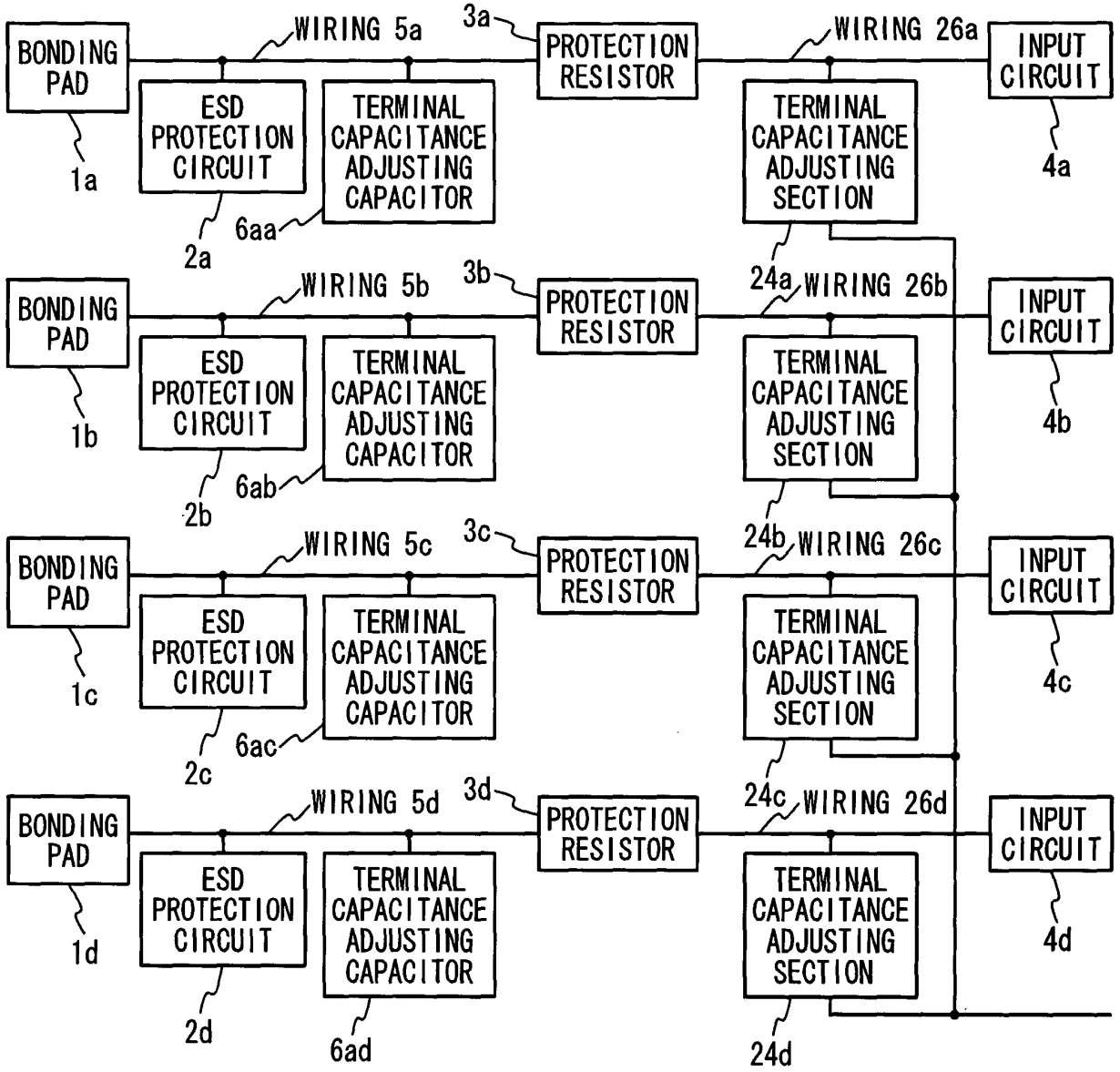

BONDING PAD
1a
WIRING 5a
3a
PROTECTION RESISTOR
WIRING 26a
INPUT CIRCUIT
4a
ESD PROTECTION CIRCUIT
2a
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6aa
TERMINAL CAPACITANCE ADJUSTING SECTION
24a
BONDING PAD
1b
WIRING 5b
3b
PROTECTION RESISTOR
WIRING 26b
INPUT CIRCUIT
4b
ESD PROTECTION CIRCUIT
2b
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ab
TERMINAL CAPACITANCE ADJUSTING SECTION
24b
BONDING PAD
1c
WIRING 5c
3c
PROTECTION RESISTOR
WIRING 26c
INPUT CIRCUIT
4c
ESD PROTECTION CIRCUIT
2c
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ac
TERMINAL CAPACITANCE ADJUSTING SECTION
24c
BONDING PAD
1d
WIRING 5d
3d
PROTECTION RESISTOR
WIRING 26d
INPUT CIRCUIT
4d
ESD PROTECTION CIRCUIT
2d
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ad
TERMINAL CAPACITANCE ADJUSTING SECTION
24d

Fig. 18

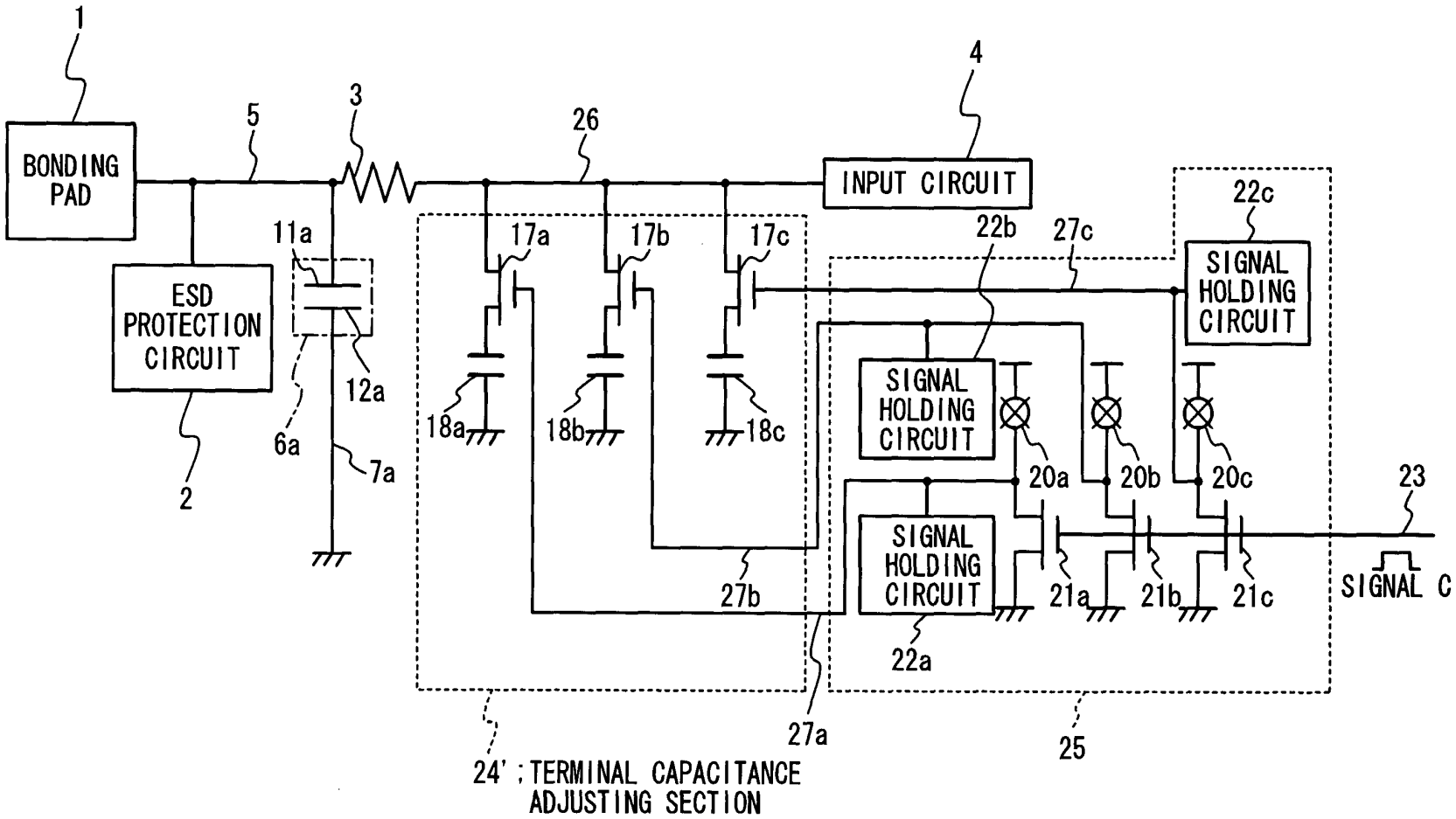

1
BONDING PAD
5
3
26
4
INPUT CIRCUIT
22c
SIGNAL HOLDING CIRCUIT
22b
27c
11a
17a
17b
17c
ESD PROTECTION CIRCUIT
12a
6a
7a
2
18a
18b
18c
SIGNAL HOLDING CIRCUIT
20a
20b
20c
23
SIGNAL HOLDING CIRCUIT
21a
21b
21c
SIGNAL C
27b
22a
27a
25
24' ; TERMINAL CAPACITANCE ADJUSTING SECTION

Fig. 19

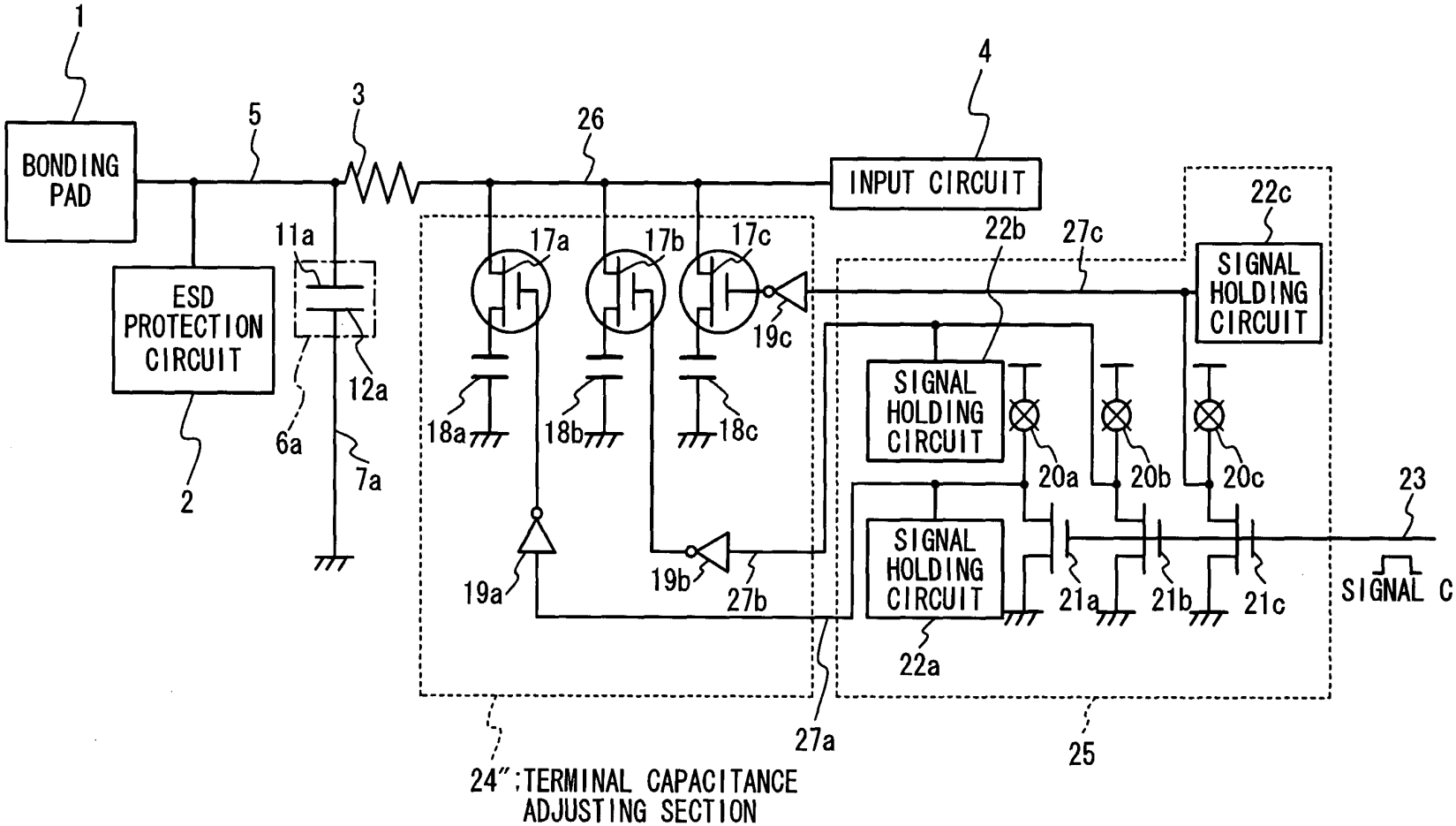

1
BONDING PAD
5
3
26
4
INPUT CIRCUIT
22c
SIGNAL HOLDING CIRCUIT
22b
27c
11a
17a
17b
17c
19c
ESD PROTECTION CIRCUIT
2
6a
12a
7a
18a
18b
18c
SIGNAL HOLDING CIRCUIT
20a
20b
20c
23
19a
19b
27b
SIGNAL HOLDING CIRCUIT
21a
21b
21c
SIGNAL C
22a
27a
25
24″:TERMINAL CAPACITANCE ADJUSTING SECTION

Fig. 20

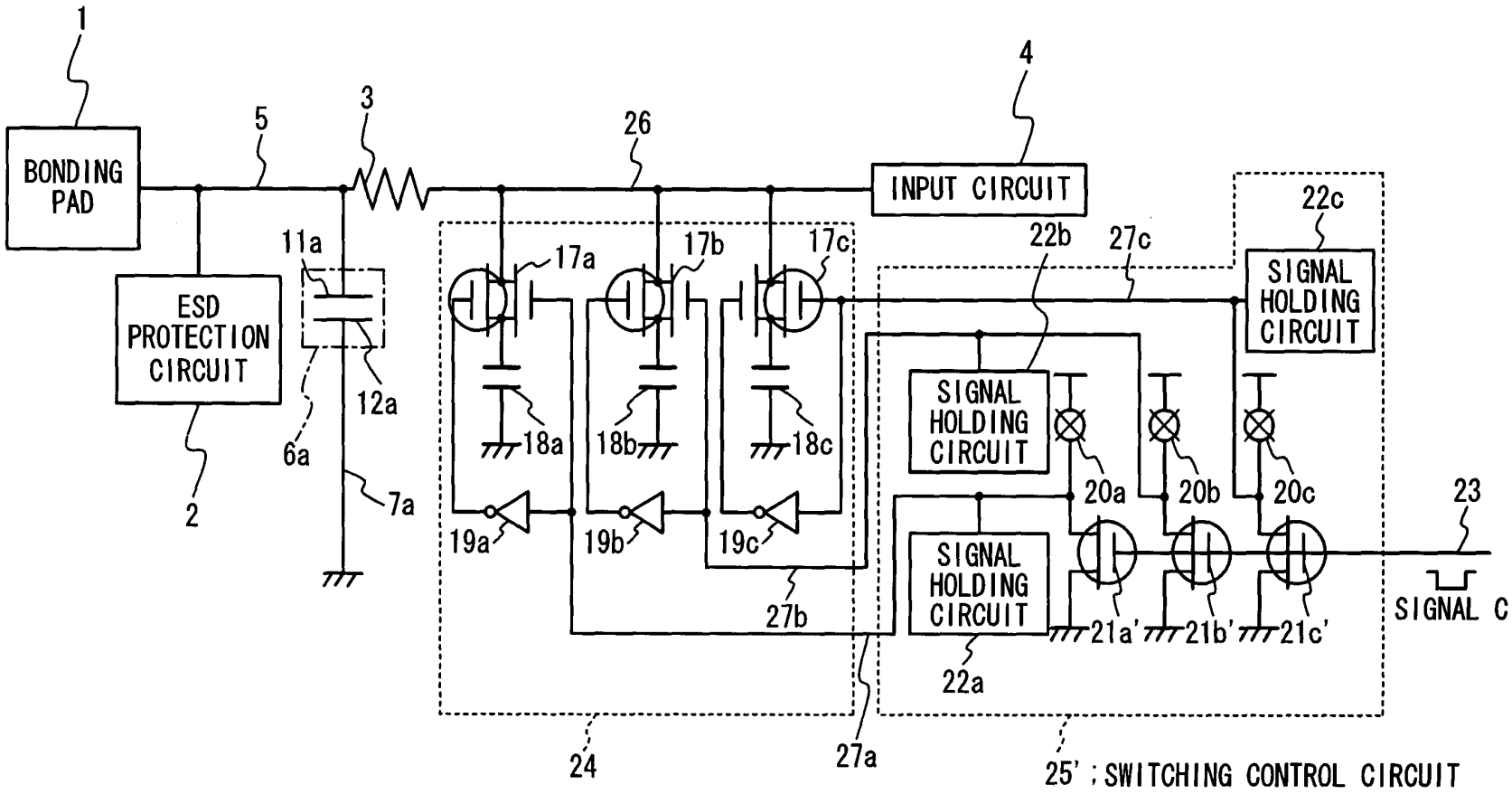

1
BONDING PAD
5
3
26
4
INPUT CIRCUIT
22c
SIGNAL HOLDING CIRCUIT
22b
27c
11a
17a
17b
17c
ESD PROTECTION CIRCUIT
12a
6a
18a
18b
18c
SIGNAL HOLDING CIRCUIT
20a
20b
20c
23
2
7a
19a
19b
19c
SIGNAL HOLDING CIRCUIT
21a'
21b'
21c'
SIGNAL C
27b
22a
24
27a
25' ; SWITCHING CONTROL CIRCUIT

Fig. 21

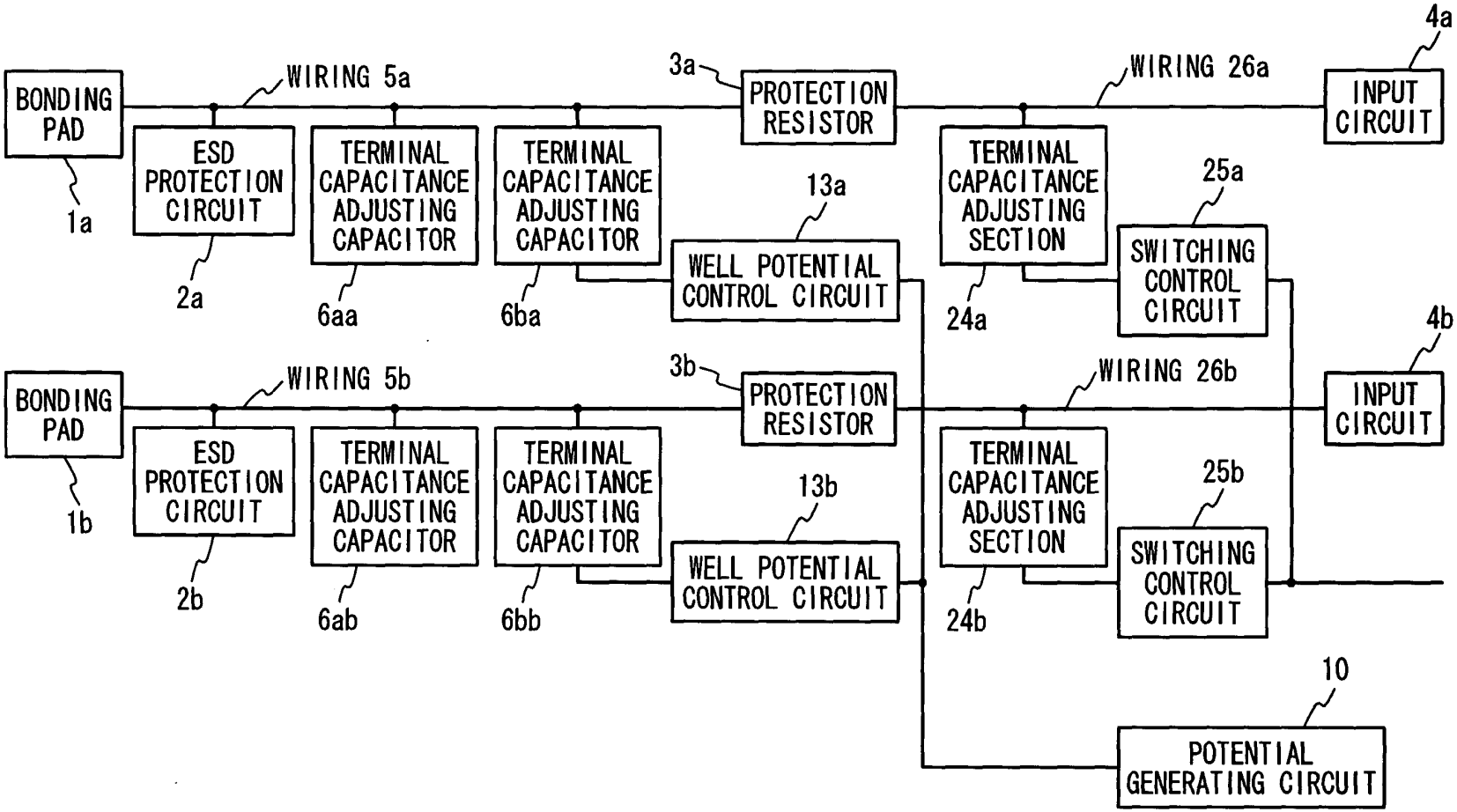
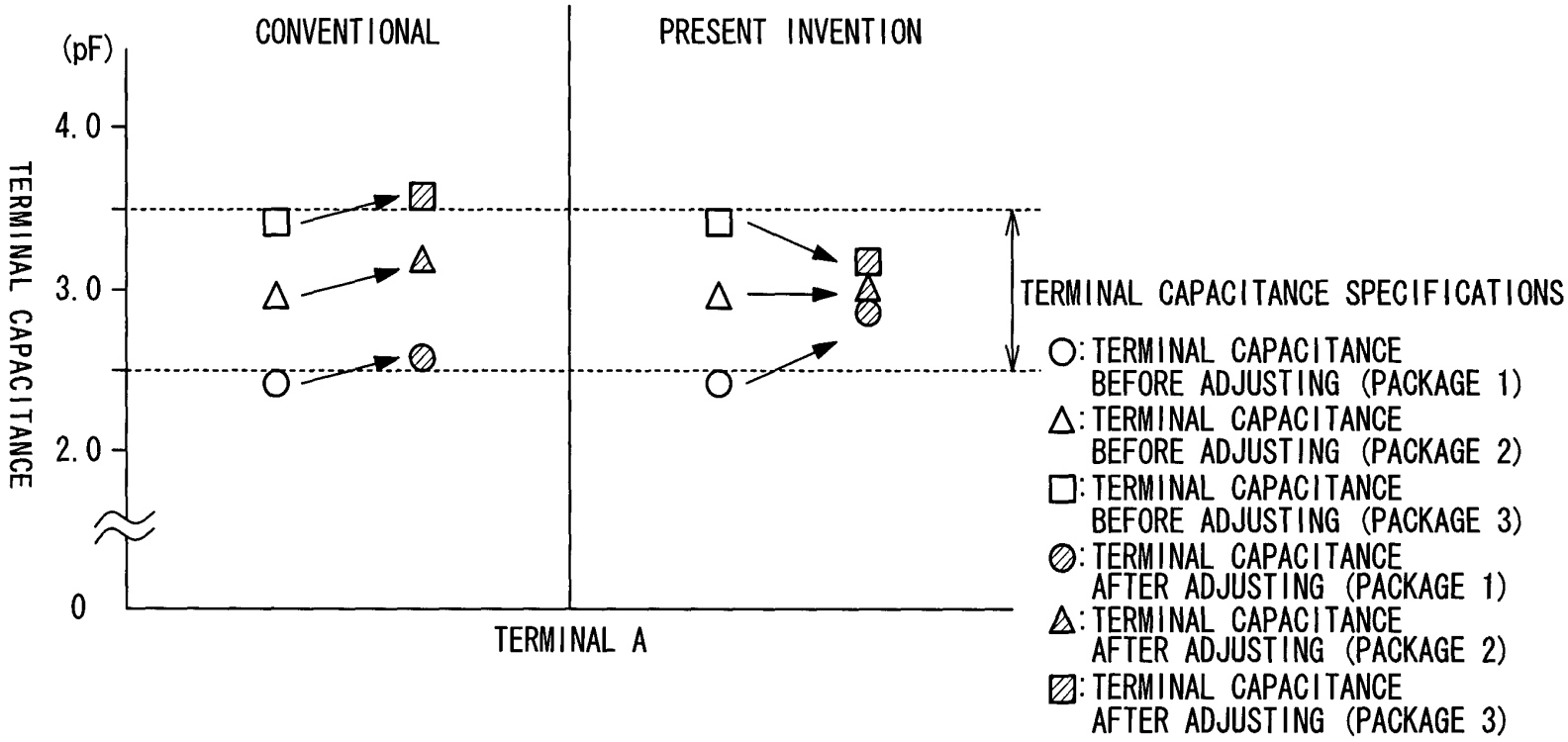

BONDING PAD
1a
WIRING 5a
ESD PROTECTION CIRCUIT
2a
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6aa
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ba
3a
PROTECTION RESISTOR
13a
WELL POTENTIAL CONTROL CIRCUIT
WIRING 26a
TERMINAL CAPACITANCE ADJUSTING SECTION
24a
25a
SWITCHING CONTROL CIRCUIT
4a
INPUT CIRCUIT
BONDING PAD
1b
WIRING 5b
ESD PROTECTION CIRCUIT
2b
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6ab
TERMINAL CAPACITANCE ADJUSTING CAPACITOR
6bb
3b
PROTECTION RESISTOR
13b
WELL POTENTIAL CONTROL CIRCUIT
WIRING 26b
TERMINAL CAPACITANCE ADJUSTING SECTION
24b
25b
SWITCHING CONTROL CIRCUIT
4b
INPUT CIRCUIT
10
POTENTIAL GENERATING CIRCUIT

Fig. 22


CONVENTIONAL
PRESENT INVENTION
(pF)
4.0
3.0
2.0
0
TERMINAL CAPACITANCE
TERMINAL A
TERMINAL CAPACITANCE SPECIFICATIONS
○: TERMINAL CAPACITANCE BEFORE ADJUSTING (PACKAGE 1)
△: TERMINAL CAPACITANCE BEFORE ADJUSTING (PACKAGE 2)
□: TERMINAL CAPACITANCE BEFORE ADJUSTING (PACKAGE 3)
⊘: TERMINAL CAPACITANCE AFTER ADJUSTING (PACKAGE 1)
▲: TERMINAL CAPACITANCE AFTER ADJUSTING (PACKAGE 2)
▨: TERMINAL CAPACITANCE AFTER ADJUSTING (PACKAGE 3)